INTRODUCTION

For any application to begin proper operation, the application must power-up properly. Many criteria must be taken into account to ensure this. The PICmicro™ devices integrate several features to simplify the design for the power-up sequence. These integrated features also reduce the total system cost.

This application note describes the requirements for the device to properly power-up, common pitfalls that designers encounter, and methods to assist in solving power-up problems.

THE POWER-UP SEQUENCE

There are several factors that determine the actual power-up sequence that a device will go through. These factors are:

- The Processor Family
  - PIC16C5X (Baseline)
  - PIC16CXXX (Midrange)
  - PIC17CXXX (High-end)
- Oscillator Configuration
- Device Configuration
- MCLR pin

The Power-on Reset (POR) signal generation is discussed, followed by the power-up sequence for the specific device families.

Power-on Reset (POR) signal

The data sheets show a Power-on Reset (POR) pulse, as in Figure 1. The POR signal is a level triggered signal. This representation may help in the understanding of future devices, which may have a brown-out reset capability.

The power-up sequence begins by increasing the voltage on the VDD pin (from 0V). If the slope of the VDD rise time is faster than 0.05 V/ms, the internal circuitry is capable of generating an internal reset signal. Depending on the device family, different power-up sequences will occur after this POR signal.

If the slope is less then 0.05 V/ms, the MCLR pin should be held low, by external circuitry, until a valid operating VDD level is reached.

The VDD rise time specification needs to be met, until the POR signal is generated. After the POR signal is generated the slope of the VDD rise can change (to a faster or slower rise). This may have other ramifications, see the "Power-up Consideration" section. In general, the POR signal will trip (PORTPR) somewhere between 1.2V to 2.0V (Figure 1).

FIGURE 1: INTERNAL POR SIGNAL

When VDD is falling, the voltage at which the internal POR signal returns to a low level is processor/device dependent. To ensure that a device will have a POR, the device voltage must return to VSS before power is re-applied.

Note: Some devices (with EPROM program memory) have a newer POR circuit that does not require VDD to return to VSS. See the device data sheet for the complete specification on the POR operation.

The POR will be generated regardless of the level of the MCLR pin. The PICmicro device families are different on what triggers the power-up sequence. Table 1 describes the events that cause the POR sequence to occur.

After reaching the POR trip point (PORTPR), the POR sequence holds the device in reset for a given time. Once this time has elapsed, the device voltage must be valid or the MCLR pin must be low. The time from the POR rising edge to the time that VDD must be valid level is the TPOR2VDV time.
TABLE 1: EVENTS THAT TRIGGER POR SEQUENCE

<table>
<thead>
<tr>
<th>Device</th>
<th>Events</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC16C5X</td>
<td>Both the POR signal rising edge and any MCLR rising edge(1)</td>
</tr>
<tr>
<td>PIC16CXXX</td>
<td>The POR signal rising edge</td>
</tr>
<tr>
<td>PIC17CXXX</td>
<td>Either the POR signal rising edge or the first MCLR rising edge (if MCLR is low when the POR occurs). After this event, all following MCLR rising edges(1) cause the device to start program execution immediately.</td>
</tr>
</tbody>
</table>

Note 1: The POR low-to-high transition onfigures Special Function Register (SFR) bits/registers to a specified value. The SFR bits/registers are not identically affected by the MCLR signal. Refer to the device data sheet to see how the bits are affected by these two conditions.

The POR sequence for each of the PICmicro families is described in the following three sections:

PIC16C5X Family
PIC16CXXX Family
PIC17CXXX Family

PIC16C5X Family

After the MCLR pin has reached a high level, the device is held in reset for typically 18 ms. This time is determined by an on-chip RC oscillator and 8-bit ripple counter. This Device Reset Timer (DRT), allows most crystals (except low frequency crystals) to start-up and stabilize. Due to the characteristics of resistors and capacitors, this time is extremely variable over temperature and voltage. There is also a device to device variation. See the data sheet for the range of this time-out.

TABLE 2: TIME-OUT IN VARIOUS SITUATIONS (TYPICAL)

<table>
<thead>
<tr>
<th>Oscillator Configuration</th>
<th>Power-up</th>
<th>Wake-up from SLEEP</th>
</tr>
</thead>
<tbody>
<tr>
<td>XT, HS, LP(1)</td>
<td>18 ms</td>
<td>18 ms</td>
</tr>
<tr>
<td>RC</td>
<td>18 ms</td>
<td>18 ms</td>
</tr>
</tbody>
</table>

Note 1: 32 kHz crystals have a typical start-up time of 1-2 seconds. Crystals >100 kHz have a typical start-up time of 10-20 ms. Resonators are typically <1 ms. All these times are voltage dependent.
PIC16CXXX Family

After the POR rising edge has occurred, the device can have up to 2 time-out sequences that occur in series. The first being the Power-up Timer (PWRT), the second being the Oscillator Start-up Timer (OST).

The Power-up Timer time-out will occur if enable bit PWRT is read as a ‘1’. The PWRT uses a 10-bit counter, with the clock from an internal RC. Due to the characteristics of resistors and capacitors, this time is extremely variable over temperature and voltage. There is also a device to device variation. See the data sheet for the range of this time-out.

The OST will occur on power-up/wake-up when the device has oscillator mode selected. This allows the oscillator to stabilize before program execution begins. The OST uses a 10-bit counter, with the clock from the OSC pin. The time is dependent on the frequency of the input clock. This timer is disabled if the oscillator is configured as RC.

Figure 3 shows how the two timers work in the power-up sequence. VDD must be valid when program execution starts. The \( TPWRT + TOST \) times can be thought of as the time that the device gives for the VDD to become valid (\( TPOR2VDDV \)). Figure 4 shows when device execution begins for the case of the MCLR pin going high before \( TPOR2VDDV \) times out. Figure 5 shows when the MCLR pin is held low longer than the \( TPOR2VDDV \) time. The device starts execution immediately when MCLR goes high. Table 3 gives typical reset times.

**TABLE 3: TIME-OUT IN VARIOUS SITUATIONS (TYPICAL)**

<table>
<thead>
<tr>
<th>Oscillator Configuration</th>
<th>Power-up ( PWRT = 1 ) (2)</th>
<th>Power-up ( PWRT = 0 ) (2)</th>
<th>Wake-up from SLEEP</th>
</tr>
</thead>
<tbody>
<tr>
<td>XT, HS, LP(^{(1)})</td>
<td>72 ms + 1024 ( T_{OSC} )</td>
<td>1024 ( T_{OSC} )</td>
<td>1024 ( T_{OSC} )</td>
</tr>
<tr>
<td>RC</td>
<td>72 ms</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Note 1: 32 kHz crystals have a typical start-up time of 1-2 seconds. Crystals >100 kHz have a typical start-up time of 10-20 ms. Resonators are typically <1 ms. All these times are voltage dependent.

2: Future devices will change the polarity of this configuration bit. Refer to the specific data sheet for the polarity of the PWRT Configuration Bit.
PIC17CXXX Family

When the MCLR pin comes to a high level, after the POR rising edge, the device has 2 time-out sequences that occur in parallel. One is the Power-up Timer (PWRT), the other is the Oscillator Start-up Timer (OST). The timer with the greater time holds the device in reset. Figure 6 shows the sequence with MCLR tied to VDD. Figure 7 shows the time-out when MCLR is independent of VDD. The PWRT time is generally longer, except for low frequency crystals/resonators. The OST time does not include the start-up time of the oscillator/resonator.

The PWRT uses a 10-bit counter, with the clock from an internal RC. The characteristics of the RC vary from device to device and over temperature and voltage. The specification for the time-out range can be found in the electrical specification of the data sheet.

The OST uses a 10-bit counter, with the clock from the OSC pin. The time is dependent on the frequency of the input clock.

Until MCLR has reached a high level, the POR sequence will not start. While the POR signal remains high, all following MCLR pulses will not cause the POR sequences to occur (Figure 8).

### TABLE 4: TIME-OUT IN VARIOUS SITUATIONS (TYPICAL)

<table>
<thead>
<tr>
<th>Oscillator Configuration</th>
<th>Power-up</th>
<th>Wake-up from Sleep</th>
</tr>
</thead>
<tbody>
<tr>
<td>RC, EC</td>
<td>Greater of 80 ms and 1024 Tosc</td>
<td>—</td>
</tr>
<tr>
<td>XT, LF(1)</td>
<td>Greater of 80 ms and 1024 Tosc</td>
<td>1024 Tosc</td>
</tr>
</tbody>
</table>

Note 1: 32 kHz crystals have a typical start-up time of 1-2 seconds. Crystals >100 kHz have a typical start-up time of 10-20 ms. Resonators are typically <1 ms. All these times are voltage dependent.

### FIGURE 6: PIC17CXX POWER-UP SEQUENCE (MCLR TIED TO VDD)

### FIGURE 7: PIC17CXX POWER-UP SEQUENCE (MCLR NOT TIED TO VDD)

### FIGURE 8: MCLR OPERATION
POWER-UP CONSIDERATIONS

The device must be at a valid operating voltage when the device exits reset. This can be done by ensuring that the power supply rise time is fast enough to guarantee an operating VDD level, or by using an external reset circuit which will hold MCLR low until the operating VDD level is reached.

When the rise time of VDD is very fast, there will be a time delay before the Power-on Reset (POR) signal will rise to a logic high (TTP2PORH). This delay is in the 1-5 µs range, as shown in Figure 9.

Figure 10, Figure 11, and Figure 12 show the maximum time from the POR sequence beginning to the device having a valid operating voltage. Table 5 gives the T POR2VDDV times. When determining the time at which VDD must be valid, the POR trip point must be assumed to be at the minimum POR voltage trip point.

How Crystal Frequencies affect Start-up time

Both the PIC16CXXX and PIC17CXXX families may have start-up times that include the contributions of the oscillator. Table 5 shows how the oscillator can affect each mode of operation, with Table 6 giving the reset time that an oscillator generates. This time can be used in the equation to calculate the total reset time, at the given frequency. This time may vary slightly due to the initial start-up characteristics of the crystal/oscillator circuit.

Note 1: The rise time specification does not ensure that a valid VDD operating voltage will be reached before the device exits reset. The device's VDD must be within the specified operating range for proper device operation.

Note 2: The start-up characteristics of the crystal/oscillator must also be taken into account when determining the time that the device must be held in reset.

TABLE 5: MAXIMUM TIME FROM POR RISING EDGE TO VALID VDD VOLTAGE

<table>
<thead>
<tr>
<th>Osc Mode</th>
<th>Maximum Time</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC16C5X LP, XT, HS, and RC</td>
<td>9 ms</td>
<td></td>
</tr>
<tr>
<td>PIC16CXXX RC</td>
<td>28 ms</td>
<td></td>
</tr>
<tr>
<td>PIC16CXXX LP, XT, and HS</td>
<td>28 ms + 1024 TOSC</td>
<td>PWRTE = 1</td>
</tr>
<tr>
<td>PIC16CXXX LP, XT, and HS</td>
<td>1024 TOSC</td>
<td>PWRTE = 0</td>
</tr>
<tr>
<td>PIC17CXXX LF, XT, EC, and RC</td>
<td>Greater of (40 ms or 1024 TOSC)</td>
<td></td>
</tr>
</tbody>
</table>

FIGURE 9: POR DELAY FOR FAST VDD RISE TIME

TABLE 6: RESET TIME DUE TO OSCILLATOR

<table>
<thead>
<tr>
<th>Clock Frequency</th>
<th>32 kHz</th>
<th>1 MHz</th>
<th>2 MHz</th>
<th>4 MHz</th>
<th>8 MHz</th>
<th>10 MHz</th>
<th>16 MHz</th>
<th>20 MHz</th>
<th>25 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>1024 TOSC</td>
<td>32 ms</td>
<td>1.0 ms</td>
<td>512 µs</td>
<td>256 µs</td>
<td>128 µs</td>
<td>102.4 µs</td>
<td>64 µs</td>
<td>51.2 µs</td>
<td>41 µs</td>
</tr>
</tbody>
</table>
FIGURE 10: MAXIMUM POWER-UP TIME, MCLR TIED TO VDD (PIC16C5X, PIC16CXXX, PIC17CXXX)

Minimum Operating VDD

Maximum POR Trip Point

Minimum POR Trip Point

VDD and MCLR

POR signal

Reset

T_{POR2VDDV}

Execution

FIGURE 11: MAXIMUM POWER-UP TIME, MCLR NOT TIED TO VDD (PIC16CXXX)

Minimum Operating VDD

Maximum POR Trip Point

Minimum POR Trip Point

VDD

MCLR

POR signal

Reset

T_{POR2VDDV}

Execution

FIGURE 12: MAXIMUM POWER-UP TIME, MCLR NOT TIED TO VDD (PIC16C5X AND PIC17CXXX)

Minimum Operating VDD

Maximum POR Trip Point

Minimum POR Trip Point

VDD

MCLR

POR signal

Reset

T_{POR2VDDV}

Execution
Oscillator and Resonator Considerations

Oscillators and resonators from different manufacturers may have different characteristics. The recommended capacitor selection can be found in each device's data sheet. When we do the capacitor selection, during the oscillator/resonator characterization, we are currently using devices from one of several manufacturers. Generally we use oscillators from either ECS, CTS, FOX or Epson, and ceramic resonators from either Murata Erie or Panasonic. Other manufacturers may be used in the future, depending on availability and other factors.

Other manufacturers devices may have significantly different characteristics. To ensure proper oscillator operation, the circuit should be verified at the lowest temperature/highest VDD (to ensure that the crystal is not overdriven), and with the highest temperature/lowest VDD (to ensure the device still starts up) that the device will be subjected to while in the application. This ensures a stable start-up and frequency for this device, at the extreme conditions of the application.

For production purposes, the above testing should be done with many different samples of the components selected. This is so the part to part variation of the capacitors, resistors, crystals/resonators, and PICmicro devices are taken into account. All PICmicro final data sheets supply the characterization information on the transconductance of the oscillator (measurement of gain). This information can be used to check part to part variations of the PICmicro.

When selecting the crystal, the designer must ensure that it is a parallel cut type. Failure to use a parallel cut crystal may cause:

- Frequency operation out of the specified range of the crystal.
- Unreliable oscillator start-up.
- Device or crystal damage.

RAM and Special Function Register Initialization

After a successful Power-up Reset, the device will begin to execute the firmware program. To have expected operation, ALL RAM should be initialized by the program. This includes the Special Function Registers (SFR) and the general purpose data memory. The use (read) of an uninitialized RAM location will cause the program to do exactly what you told it, with the unexpected RAM value. It should not be expected that all devices will power-up with the same uninitialized device values.

There are many factors that contribute to how a RAM cell powers up, but the most common “gotcha” is between the Windowed and OTP device types. Many times a user forgets to cover the window after erasing the Windowed device. When the device is powering up, and the light is able to shine onto the device die, the transistor characteristics will shift. This can cause the device RAM to have a different power-up value than a device where no light can shine onto the die (OTP or covered).

Note: RAM locations should be initialized before they are used. Use of an uninitialized location will cause proper device operation with the improper values. That is, it will do what you told it to do, not what you wanted it to do.

Valid Operating Voltage Levels

When the device is operating, the device voltage must be within the specified Min/Max limits. Operation of the device outside these limits may cause unexpected device operation.

One of the primary functional failure modes of a device is when the applied voltage is lower than the specified minimum requirement. This functional failure is called Brown-out. Brown-out causes the program memory not to be read correctly. For example, the program counter may be pointing to a MOVE instruction, but the device reads it as a GOTO instruction (with a random destination). This can have disastrous affects to the operation of the application. If brown-out conditions are possible, the application needs to be protected by using a brown-out circuit. A brown-out circuit works with the MCLR pin to put the device in RESET before the device’s actual voltage violates the minimum limit.

Figure 13 shows a low cost external brown-out protection circuit. The voltage at which the circuit causes a reset is dependent upon the tolerances of the components. Figure 14 shows the use of a Dallas Semiconductor EconoReset. This device monitors the status of the power supply, and generates a reset when an out-of-tolerance condition is detected. Motorola also makes some 3-terminal devices to monitor the power supply, such as the MC34164, MC34064, MC33064. Their data sheets should be reviewed to ensure that the device is suitable for your application.
Brown-out and the WDT

The recommended solution for brown-out conditions is the use of a brown-out circuit. The brown-out circuit will keep the device in reset until a valid operating voltage is present. In some applications the additional cost of the external brown-out circuit, can be traded-off with system recovery from brown-out. Use of the Watchdog Timer (WDT) can enhance the probability of system recovery from a brown-out condition.

Note: If I/O drive conflicts can cause critical problems, this technique should not be used. This is due to the indeterminate time before a device reset could occur, which would reset all pins to inputs to eliminate any I/O conflict.

When using the WDT in brown-out conditions, care must be taken. Brown-outs may cause an unrecoverable condition, but with good design practice the probability of this can be significantly reduced.

During a brown-out, improper program execution can occur due to an EPROM read failure. This program execution can also corrupt data memory locations, which include the Special Function Registers (SFRs). Corrupting the control registers may cause hardware conflicts. For example, an input may become an output. Other conflicts are possible, but the situation will be application dependent.

As the device voltage gets lower, internal logic can become corrupted. This can include the Program Counter (PC) value, Stack Pointer and contents, State machines, Data Memory, etc.

When a valid voltage is returned, the device may be at an unexpected program location, possibly using corrupted values. In this situation, the device would not be expected to operate as intended and could get into a state that appears locked-up.

For the PIC17C42 in code protected microcontroller mode, once the Program Counter (PC) exceeds the 32K-word boundary, the device will become locked-up. The PC can exceed the 32K-word boundary from the execution of incorrect instructions (due to failure reading the EPROM) or by the PC becoming corrupted.

If the WDT is to be used to reset the device, care must be used in structuring the program. Optimally, only one CLRWDT instruction should be used. This minimizes the possibility of program execution returning to a loop which clears the WDT. This loop could then lock-up the device, since other control registers are corrupted and the device is not configured as expected. An example is; if the loop was waiting for an interrupt, but the bit that enables global interrupts was disabled, the device would no longer respond to the interrupts and would appear locked-up.

Example 1 shows a simple implementation of using the WDT reset for system recovery. The program loops, waiting for a WDT time-out (which clears the T0 bit). After the WDT reset, the T0 bit needs to be set (by executing a CLRWDT instruction). The program should then initialize the device. Then application code can start executing. There is a possibility of the T0 bit being corrupted by low voltage, and the device not being in a reset state when the software initializes the device.

The WDT example in Appendix B: uses a different method, independent of the T0 bit. This uses RAM locations which get loaded with a value. A WDT time-out (or other reset) needs to occur. The RAM locations are verified to contain the same values. Once the RAM is verified, it is cleared, and the device should be initialized. These RAM locations can be used by the application program.
EXAMPLE 1: USING WDT RESET

```
org  Reset_Address
GOTO  TO_TEST ;At any reset,
         ;test the TO bit
org  TO_TEST
BTFSC STATUS, TO  ;WDT Time-Out?
HERE GOTO HERE ;NO, Wait for TO
Time_Out  ;YES, Good Reset
CLRWDT  ;Start here
:        ;Initialize Device
:        ;Application Code
```

False Power-down

In applications where power is removed from the device's supply lines, but voltage is still applied to an I/O pin, unexpected operation may occur. Power is able to be supplied to the device through this I/O pin. Since the device is still partially powered, the internal logic is never completely powered down. Figure 15 shows the general structure of an I/O pin. Figure 16 depicts the internal voltage level that is actually applied to some device logic, versus what is seen at the pin.

To guarantee a Power-on Reset (POR) rising edge, the device voltage (VDD) must start from VSS. When the device is inadvertently powered from an I/O pin, the voltage at the VDD pin may appear to be near ground but may actually be higher in the device. With some of the internal logic powered, the characteristics of the device can be similar to a brown-out situation. Similar design practices to brown-out should be implemented.

A method for protecting the device from being powered from an I/O pin is shown in Figure 17.

FIGURE 15: TYPICAL ELECTRICAL STRUCTURE OF I/O PIN
TROUBLESHOOTING

There are several techniques that can be used to troubleshoot problems related to powering up. First it is important to try to locate the source of the problem. These sources could be:

- No oscillation on OSC1/OSC2 pins
- Improper/no Program Execution

In cases where there is no oscillation on the OSC1/OSC2 pins, some of the following should be tried:

a) Verify that there are good connections/the components are good.
b) Verify that the crystal/resonator manufacturer is one that has been tested, if not try other capacitor values.
c) See if an external clock (from a function generator) causes device operation to begin.
d) Verify that all components are well grounded.
e) If a scope probe is connected to the oscillator output, it must be a low capacitance/high impedance probe. If it is not, the oscillator may stop.

In cases where program execution is not as expected:

a) Use a minimal program with external clock input.
b) Tie MCLR to ground until solid power is applied to the device then release MCLR (bring high).
c) Measure VDD rise time to determine if an external reset circuit is needed, and, if so, what type of reset circuit should be used.
d) Verify that the device program memory and configuration bits are programmed to their expected states.

The flowchart shown in Figure 18 can be used to troubleshoot power-up problems. This flowchart is only intended to be the first level diagnostic in trying to solve a power-up problem. Many other flowcharts can be used, depending on the characteristics of the problem and the set-up of the application.

CONCLUSION

Understanding the criteria for the powering up of a device will allow you to make better design choices. If device power-up problems are still encountered, many techniques can be used to solve the problem. Appendix B contains example code which can be used to verify that a device is operating (powered-up correctly). This eliminates the possibility of the program as the cause, and allows debug on the hardware.
FIGURE 18: TROUBLESHOOTING FLOWCHART

- OSC output is not over/under driven
- Capacitors are at their proper values
- The oscillator/resonator gives the desired value
- The optional series resistor is a proper value
- All components are well grounded

Check the following:
- OSC output is not over/under driven
- Capacitors are at their proper values
- The oscillator/resonator gives the desired value
- The optional series resistor is a proper value
- All components are well grounded

Try using an External Clock (select proper bit option for external clock)

Suspect device, programmer or circuit

Isolate device pins from voltage

Suspect software

Does minimal program work? (Appendix B)

Try using an External Clock (select proper bit option for external clock)

Suspect device, programmer or circuit

Isolate device pins from voltage

Suspect software

Check the following:
- OSC output is not over/under driven
- Capacitors are at their proper values
- The oscillator/resonator gives the desired value
- The optional series resistor is a proper value
- All components are well grounded

Try using an External Clock (select proper bit option for external clock)

Suspect device, programmer or circuit

Isolate device pins from voltage

Suspect software

Does minimal program work? (Appendix B)

Try using an External Clock (select proper bit option for external clock)

Suspect device, programmer or circuit

Isolate device pins from voltage

Suspect software

Check the following:
- OSC output is not over/under driven
- Capacitors are at their proper values
- The oscillator/resonator gives the desired value
- The optional series resistor is a proper value
- All components are well grounded

Try using an External Clock (select proper bit option for external clock)

Suspect device, programmer or circuit

Isolate device pins from voltage

Suspect software

Does minimal program work? (Appendix B)

Try using an External Clock (select proper bit option for external clock)

Suspect device, programmer or circuit

Isolate device pins from voltage

Suspect software

Check the following:
- OSC output is not over/under driven
- Capacitors are at their proper values
- The oscillator/resonator gives the desired value
- The optional series resistor is a proper value
- All components are well grounded

Try using an External Clock (select proper bit option for external clock)

Suspect device, programmer or circuit

Isolate device pins from voltage

Suspect software

Does minimal program work? (Appendix B)
APPENDIX A: Q & As

Q. When I use a windowed device (JW), my application works as expected. When I program an OTP device, it no longer works as expected. Why is this?

A. The silicon is the same between the OTP and windowed devices. If the windowed device’s window is not covered (with black tape), light shines onto the silicon. The light causes the potential levels of gates to shift. This in turn can cause RAM to be initialized to an unknown state, which could be different than in the OTP device. If RAM is not initialized by the program before it is used, these different power-up states of the RAM could be the cause of the problem. Ensure that all RAM is initialized in the device. This includes the SFRs.

Q. My oscillator is not oscillating, what could be wrong?

A. There are several possibilities, some which include:
   1. The wrong oscillator bit setting is selected. The erased (default) state is RC oscillator mode.
   2. The wrong capacitor values are installed. Refer to the most current data sheet for recommended values.
   3. The characteristics of your manufacturers crystal are different than those that are characterized by Microchip. Generally our tests have been done with one of the following manufacturers’ crystals/resonators: ECS, FOX, Murata Erie, or Panasonic.
   4. The external connections to the device are wrong. Verify that all connections to the device are correct and that good signals/levels are being applied.
   5. The cut of the crystal is a series type, as opposed to the specified parallel type.
   6. No bypassing capacitors were used on the device. The noise on VDD could be affecting the oscillator circuitry.

Q. The device was powered-down and then powered back up, but the device does not operate. What could be wrong.

A. Possibilities include:
   1. If power was applied to an I/O pin when the device was “powered-down”, the device would be powered through the I/O pin. The internal logic is not actually powered-down, and Power-on Reset (POR) will not occur.
   2. When VDD was powered-down, VDD was not given enough time to settle to 0V.
   3. The VDD ramp rate is too slow.

Q. My oscillator is oscillating, but the device is not working. What could be wrong?

A. There are several possibilities, some which include:
   1. Slow VDD rise time, which was too slow to cause a Power-on Reset (POR). The rise time should not exceed the minimum device specification. For most devices this is 0.05 V/ms. Also the device must be at the minimum operating VDD of the processor when reset is exited.
   2. Ensure that the MCLR pin is not low. This holds the device in RESET.
   3. A brown-out has occurred, and has corrupted the internal state machines (including the WDT). An external brown-out circuit is recommended to hold the device in RESET during the brown-out condition.
   4. The CLRWDT instruction is not being used (often enough) when the WDT is enabled.

Q. When I power-up the device, it does not operate and it gets hot.

A. Your design is probably permitting fast high voltage signals (spike) onto one of the device pins. This sudden high voltage (and associated current) is in excess of the protection diode limit. The device must be powered-down (to Vss) to release this condition. This condition may cause a functional failure or affect device reliability. All Microchip devices meet or exceed the Human Body Model (HBM) and Machine Model (MM) for ESD and latch-up.
Q. My oscillator is oscillating, but not at the expected frequency. What could be wrong.

A. For many designers, working with oscillators and their related issues are a “black magic”, since the characteristics can vary widely between manufacturers. I suggest that you read all the application notes that we have available on oscillators. Some quick possibilities are:

1. The cut of the crystal is a series type, as opposed to the specified parallel type.
2. No bypassing capacitors were used on the device. The noise on VDD could affect the oscillator circuitry.
3. The capacitor values used are causing the oscillator to operate in one of the harmonic frequencies.

Note: This is not an all inclusive list. You may need to investigate other design aspects.

Q. The device seems to never exit reset, or is continually resetting.

A. The CLRWDT instruction is not being used (often enough) when the WDT is enabled.

Q. The device was powered-down and back up again, but it does not reset. It just starts operating immediately.

A. Possibilities include:

1. If power was applied to an I/O pin when the device was “powered-down”, the device would be powered through the I/O pin. The internal logic is not actually powered-down, and a Power-on Reset (POR) will not occur.
2. When VDD was powered down, VDD was not given enough time to settle to 0V.

Q. The oscillator is operating (I check it with a scope), yet when I look at other pins the program is not executing. Why?

A. One possible reason is that when the oscilloscope probe is placed on the OSC2 pin, the additional capacitance is enough to cause oscillation to start. Removing the capacitive load of the probe causes the oscillation to stop.
APPENDIX B: TEST PROGRAMS

PIC16C5X BIT TOGGLE

LOC    OBJECT CODE     LINE SOURCE TEXT
VALUE

0001 LIST P = 16C54, F = INHX8M, n = 66
0002 ;
0003 ;********************************************************************
0004 ; This program is a minimum program to toggle a single I/O port pin for the
0005 ; 16C5x family of devices. The only initialization is that of the data
0006 ; direction register (TRIS) of the I/O pin and the Toggling of the pin.
0007 ; The waveform will be 1 unit high and 3 units low.
0008 ;
0009 ; Program:      C5X_B0T.ASM
0010 ; Revision Date: 12-20-94
0011 ;****************************************************************************
0012 ;**************************************************************************
0013 ;****************************************************************************
0014 ; HARDWARE SETUP
0015 ;       None
0016 ;****************************************************************************
0017 ;INCLUDE <p16C5x.inc>
0018 ;****************************************************************************
0019 ;*****      Start program here.
0020 ;****************************************************************************
0021;
0022 OFF9 __FUSES ( _CP_OFF & _WDT_OFF & _XT_OSC )
0023;
0024 ;****************************************************************************
0025 ;**** Start program here.
0026 ;****************************************************************************
0027 0000 0028 START      ; POWER_ON Reset (Beginning of program)
0028 0000 0063 CLRIF STATUS ; Do initialization (Bank 0)
0029 0001 0C00 MOVLW 0x00 ; Specify value for PortB output latch
0030 0002 0026 MOVWF PORTB ;
0031 0003 0C00 MOVLW 0x00 ; Specify which PortB pins are inputs / outputs
0032 0004 0006 TRIS PORTB ;
0033 0034 0005 0506 lzz BSF PORTB, 0 ; B0 is High
0035 0006 0406 BCF PORTB, 0 ; B0 is Low
0036 0007 0A05 GOTO lzz ; Loop
0037 0038 ;
0039 0040 ;
0041 ; Reset address. Determine type of RESET
0042 ;****************************************************************************
0043 0043 IFDEF __16C54
0044 0045 RESET_V EQU 0x1FF
0046 IFDEF __16C54A
0047 0048 RESET_V EQU 0x1FF
0048 IFDEF __16C54A
0049 ENDIF
0050 IFDEF __16C55
0051 0052 RESET_V EQU 0x1FF
0052 IFDEF __16C55
0053 ENDIF
0054 IFDEF __16C56
0055 0056 RESET_V EQU 0x1FF
0056 IFDEF __16C56
0057 ENDIF
0058 IFDEF __16C57
0059 0060 RESET_V EQU 0x1FF
0060 IFDEF __16C57
0061 ENDIF
0062
MEMORY USAGE MAP ('X' = Used, '−' = Unused)

0000 : XXXXXXXX-------- ---------------- ---------------- ----------------
0040 : ---------------- ---------------- ---------------- ----------------
0180 : ---------------- ---------------- ---------------- ----------------
01C0 : ---------------- ---------------- ---------------- --------------XX

All other memory blocks unused.

Errors : 0
Warnings : 0
Messages : 0
This program is a minimum program to toggle a single I/O port pin for the 16Cxx family of devices. The only initialization is that of the data direction register (TRIS) of the I/O pin and the Toggling of the pin. The waveform will be 1 unit high and 3 units low.

**HARDWARE SETUP**

INCLUDE <p16Cxx.inc>

<table>
<thead>
<tr>
<th>LOC</th>
<th>OBJECT</th>
<th>CODE</th>
<th>LINE</th>
<th>SOURCE</th>
<th>TEXT</th>
</tr>
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0071 PROG_MEM_END EQU 0x7FF
0072 ENDIF
0073 ;
0074 IFDEF __16C65
0075 PROG_MEM_END EQU 0xFFF
0076 ENDIF
0077 ;
0078 IFDEF __16C84
0079 PROG_MEM_END EQU 0x3FF
0080 ENDIF
0081 ;
0082 IFDEF __16C84A
0083 PROG_MEM_END EQU 0x3FF
0084 ENDIF
0085 ;
0086 ;
0087 org PROG_MEM_END ; End of Program Memory
0088 ERR_LP_1 GOTO ERR_LP_1 ; If you get here your program was lost
0089 ;
0090 ;
0091 end
0092
0093
0094
0095

MEMORY USAGE MAP ('X' = Used, '-' = Unused)

0000 : XXXXXXXXXXX------ ---------------- ---------------- ----------------
0040 : ---------------- ---------------- ---------------- ----------------
0F80 : ---------------- ---------------- ---------------- ----------------
0FC0 : ---------------- ---------------- ---------------- ---------------X
All other memory blocks unused.

Errors : 0
Warnings : 0
Messages : 0

Note: Special Function Register data memory locations, in Bank 1, are specified by their true address in the file PIC16CXXX.INC. The use of the MPASM assembler will generate a warning message, when those labels are used with direct addressing. Warning messages can be turned off with an assembler option.
PIC17CXXX BIT TOGGLE

MPASM 01.02.04 Intermediate  P17_B0T.ASM  12-19-1994  17:15:3                PAGE  1

LOC  OBJECT CODE     LINE SOURCE TEXT
     VALUE

0001 ; LIST    F = 17C42,  F = INHX32,  n = 66
0002 ;
0003 ;******************************************************************************
0004 ;
0005 ; This program is a minimum program to toggle a single I/O port pin for the
0006 ; 17Cxx family of devices. The only initialization is that of the data
0007 ; direction register (DDR) of the I/O pin and the Toggling of the pin.
0008 ; The waveform will be 1 unit high and 1 unit low.
0009 ;
0010 ;    Program:         P17_B0T.ASM
0011 ;    Revision Date:   12-20-94
0012 ;
0013 ;******************************************************************************
0014 ;
0015 ; HARDWARE SETUP
0016 ;
0017 ; INCLUDE <p17Cxx.inc>
0018 ;
0019 ; FF02       __FUSES ( _MC_MODE & _WDT_NORM & _XT_OSC )
0020 ;
0021 ;*****************************************************************************
0022 ;*****      Start program here.
0023 ;*****************************************************************************
0024 ;
0025 ; START                               ; POWER_ON Reset (Beginning of program)
0026 ;
0027 ;
0028 ;
0029 ;
0030 ;
0031 ;
0032 ;
0033 ;
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0035 ;
0036 ;
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0048 ;
0049 ;
0050 ;
0051 ;
0052 ;
0053 ;
0054 ;
0055 ;

MEMORY USAGE MAP ('X' = Used,  '-' = Unused)

0000 : XXXXXXXX-------- ---------------- ---------------- ----------------
0040 : ---------------- ---------------- ---------------- ----------------
0078 : ---------------- ---------------- ---------------- ---------------X

All other memory blocks unused.

Errors :  0
Warnings :  0
Messages :  0
WDT RESET WITH RAM VERIFY

MPASM 01.20 Released
016CXX.ASM 6-30-1995 16:04:36 PAGE 1

LOC  OBJECT CODE  LINE SOURCE TEXT
VALUE

00001 LIST  P = 17C44,  F = INHX32, n = 66
00002 ;
00003 ;****************************************************************************
00004 ;
00005 ; This program is a minimum program to recover from a brown-out condition thru
00006 ; the use of the WDT. The method is to load RAM locations with a known value
00007 ; and compare these locations after any RESET. If the RAM location matches the
00008 ; expected value then program flow can continue. The longer this RAM string
00009 ; is, the greater the probability that the RAM would NOT power up in that state.
00010 ;
00011 ;
00012 ; NOTE: This does not Guarantee device recovery, due to the random start-up
00013 ; point after brown-out. This point could be a loop with a CLRWD
00014 ; instruction. The recommended solution is to always use a brown-out
00015 ;
00016 ;
00017 ; Program:  B0_RAMT.ASM
00018 ; Revision Date:  06-29-95
00019 ;
00020 ;****************************************************************************
00021 ;
00022 ;
00023 ; HARDWARE SETUP
00024 ;
00025 ;
00026 ;

00027 TRUE  EQU  1
00028 FALSE  EQU  0

00030 Debug  EQU  TRUE
00031 #define __CONFIG __FUSES
00032 ;
00033 INCLUDE <DEV_FAM.inc>
00102 list
00034 ;
00035 if ( P16C5X )
00036 INCLUDE <p16C5x.inc>
00037 __CONFIG ( _CP_OFF & _WDT_ON & _XT_OSC )
00038 endif
00039 ;
00040 if ( P16CXX )
00041 INCLUDE <p16Cxx.inc>
00042 __CONFIG ( _CP_OFF & _WDT_ON & _XT_OSC & _PWRTE_ON )
00043 endif
00044 ;
00045 if ( P17CXX )
00046 INCLUDE <p17Cxx.inc>
00047 LIST
00048 ;
00049 ; P17CXX.INC Standard Header File, Version 2.01 Microchip Technology, Inc.
00050 list
00298__CONFIG ( _MC_MODE & _WDT,NORM & _XT_OSC )
00051 ;
00052 endif
00053 ;
00054 if ( P16C5X + P16CXX + P17CXX != 1 )
00055 MESSG "WARNING - USER DEFINED: One and only one device family can be selected"
00056 endif
00057 ;
00058 ;****************************************************************************
00059 ;*****      Start program here.
00060 ;****************************************************************************
00061 ;
00062 org  Reset_Address  ; in the LIST directive
00063 ;
00064 if ( P16C5X )
00065 org 0h  ; Override the start of this code.
00066 CLRF STATUS  ; Force program memory to Page 0
00067 CLRF FSR  ; Force Data Memory to Bank 0
00068 endif

© 1997 Microchip Technology Inc.
00069 ;
00070   if ( P16CXX )
00071       CLR PCLATH ; Force program memory to Page 0
00072   endif

00073 ;
00074 ;
00075   if ( P17CXX )
00076       CLR PCLATH, F ; Force program memory to Page 0
00077   endif

00078 ;
00079 ;
00080   GOTO RAM_TEST ; At any reset,
00081       ; test the RAM

00082 ; In RAM_TEST, program execution is held-off until a valid "warm" reset
00083 ; occurs. That is, the contents of some RAM locations retain the
00084 ; values that were written to them. The probability that the RAM would power-up
00085 ; in that state is dependent on the number of bytes of RAM used. The
00086 ; more RAM, the less the probability (probability = 1 / ( 2 ** 8(N+1) ).
00087 ;
00088 ;
00089 ;
0100   org MAIN ; In Program Memory Page 0
0100 00090 00100 RAM_TEST
0101 00091 00101 0100 B0A5
0102 00092 00102 0100 0520
0103 00093 00103 0100 9204
0104 00094 00104 0100 C110
0105 00095 00105 0100 090F
0106 00096 00106 0100 9204
0107 00097 00107 0100 C110

00110 ;
00111   if ( P16C5X || P16CXX )
00112     CLR RAM0 ; YES, Time-out
00113     CLR RAM1 ; occurred, clear
00114   ;
00115     CLR RAMn ;
00116   endif

00117 ;
00118 ;
00119   if ( P17CXX )
00120     CLR RAM0, F ; YES, Time-out
00121     CLR RAM1, F ; occurred, clear
00122   ;
00123   ;
00124     CLR RAMn, F ;
00125   endif

00126 ;
00127 010C 2920
00128 010D 2921
00129 010E 2922
00130 010F 9204
00131 010G C117

00132 ;
00133 0110 0004
00134   CLRWDT ; YES, Good Reset
00135 ;
00136 ;
00137 ;
00138   GOTO HERE ; Wait for WDT TO
00139   GOTO HERE ;
00140 ;
00141 ;
00142 ;
00143 ;
00144 if ( Debug ) ;
00145   if ( P16C5X )

00146     CLR PORTB ; PORTB output latch is cleared
00147     MOVLW 0x00 ;
00148     TRIS PORTB ; Port B is output
00149     BCF PORTB, 0 ;
00150     BCF PORTB, 0 ; Toggle pin B0
00151   endif

00152 ;
00153 ;
00154 ;
00155 ;
00156 ;
00157 ;
00158 ;
00159 ;
if ( P16CXX )
    CLRF PORTB        ; PORTB output latch is cleared
    BSF  STATUS, RP0  ; Bank 1
    CLRF TRISB        ; Port B is output
    BCF  STATUS, RP0  ; Bank 0
    BCF  PORTB, 0     ;
    BSF  PORTB, 0     ; Toggle pin B0
endif

if ( P17CXX )
    CLRF PORTB, F    ; PORTB output latch is cleared
    CLRF DDRB, F     ; Port B is output
    BCF  PORTB, 0    ;
    BSF  PORTB, 0    ; Toggle pin B0
endif

endif
GOTO Time_Out         ; Return to start of Program
org PROG_MEM_END      ; End of Program Memory
ERR_LP_1
GOTO ERR_LP_1         ; If you get here your program was lost
if ( P16C5X )
    NOP                      ; This will cause the Program memory rollover
    ; for PIC16C5x devices
endif

end

MEMORY USAGE MAP ('X' = Used, ' ' = Unused)

0000 : XXX------------- ---------------- ---------------- ----------------
0040 : ---------------- ---------------- ---------------- ----------------
0100 : XXXXXXXXXXXXXXX XXXXXXXXXXXXXX-- ---------------- ----------------
0140 : -- ----------- ---------------- ---------------- ----------------
1F80 : ---------------- ---------------- ---------------- ---------------X
1FC0 : ---------------- ---------------- ---------------- ----------------
FE00 : X--------------- ---------------- ---------------- ----------------
FE40 : ---------------- ---------------- ---------------- ----------------

All other memory blocks unused.

Errors :  0
Warnings :  0
Messages :  0
Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable".
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

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